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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/748,995	12/30/2003	Hong-Jyh Li	2003 P 54309 US	8237

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EXAMINER	
KANG, DONGHEE	
ART UNIT	**PAPER NUMBER**
2811	

DATE MAILED: 04/27/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

AK

Office Action Summary	Application No.	Applicant(s)	
	10/748,995	LI, HONG-JYH	
	Examiner	Art Unit	
	Donghee Kang	2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *15 April 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-32* is/are pending in the application.

4a) Of the above claim(s) *17-32* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2,4-11 and 13-16* is/are rejected.

7)☒ Claim(s) *3 and 12* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *30 December 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *12/30/03&02/10/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

1. Claims17-32 are withdrawn from further consideration pursuant to 37 CFR 1.142(b) as being drawn to a nonelected Invention, there being no allowable generic or linking claim. Election was made **without** traverse in the reply filed on 04-15-05.

Information Disclosure Statement

2. Acknowledgment is made of receipt of applicant's Information Disclosure Statement (PTO-1449) field December 30, 2003 & February 10, 2004.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 1-2 & 4-5 are rejected under 35 U.S.C. 102(b) as being anticipated by Takagi (US 6,472,685).

Re claim 1, Takagi teaches a method of fabricating a transistor, the method comprising (Fig.3):

providing a workpiece (10); growing a stressed semiconductor layer (12) over the workpiece; growing a first layer of silicon and carbon (13) over the stressed semiconductor layer; depositing a gate dielectric material (15) over the layer of silicon and carbon; depositing a gate material (16) over the gate dielectric material; patterning the gate material and gate dielectric material to form a gate and a gate dielectric

disposed over the layer of silicon and carbon; and forming a source and a drain region (17-18) in the layer of silicon and carbon and stressed semiconductor layer, wherein the source region, drain region, gate, and gate dielectric comprises a transistor. See also Col.9, lines 27-49.

Re claim 2, Takagi teaches growing the layer of silicon and carbon comprises epitaxially growing a layer of about 90 to 99.5 % silicon and about 0.5 to 10 % carbon having a thickness 10 nm which is in the claimed ranges.

Re claim 4, Takagi teaches depositing the gate dielectric material comprises an oxide and the gate material comprises a polysilicon.

Re claim 5, Takagi teaches the method further comprising depositing a thin semiconductor material (14) over the first layer of silicon and carbon, before depositing the gate dielectric material.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claim 6 is rejected under 35 U.S.C. 103(a) as being unpatentable over Takagi (US 6,472,685).

Takagi teaches the thin semiconductor material comprises Si but thickness of Si. It is an obvious matter of routine experimentation to find the optimal thickness ranges. Generally, difference in thickness will not support the patentability of subject matter

encompassed by the prior art unless there is evidence indicating such thickness is critical.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to select the thickness of the silicon layer, since it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or workable ranges involves only routine skill in the art. *In re Aller*, 105 USPQ 233.

7. Claims **7-11 &13-16** are rejected under 35 U.S.C. 103(a) as being unpatentable over Takagi (US 6,472,685) in view of Yu et al. (US 6,784,101).

Re claims 7 & 15, Takagi teaches the method further comprising forming isolation regions (Fig.8) in the workpiece, before or after growing the stressed semiconductor layer over the workpiece and growing a first layer of silicon and carbon over the workpiece, but forming spacers over sidewalls of the gate and gate dielectric.

Yu teaches forming spacer (10, Fig.6) over sidewalls of the gate and gate dielectric to provide a protection.

Therefore, it would have been obvious to one fo ordinary skill in the art at the time the invention was made to form spacers over sidewalls of the gate and gate dielectric to provide a protection as taught by Yu in Takagi's method in order to provide a protection for gate electrode from environmental damages.

Re claims 8 & 16, Takagi soes not teach the workpiece comprises providing a silicon-on-insulator (SOI) wafer. Yu teaches forming transistor on Si wafer or SOI

substrate (Col.6, lines 56-57). It is well known in the art that SOI technology allows the formation of high-speed, shallow-junction device. In addition, SOI improves performance by reducing parasitic junction capacitance. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to form the transistor on SOI substrate since SOI improves performance of transistor by reducing parasitic junction capacitance.

Re claims 9-11 & 13, Takagi teaches substantially the entire claimed method, as explained in section 4, except that the gate dielectric and gate material comprise a high-dielectric constant material and metal, respectively. Yu teaches using a high dielectric constant material and metal as a gate insulating layer and gate electrode, respectively (Col.8, lines 15-19). Yu noted high-k dielectric material replace the conventional silicon oxide-based low-k dielectric materials. The increased capacitance k of the gate dielectric material advantage results in an increase in the gate-to-channel capacitance, which in turn results in improved device performance (Col. 2, lines 17-23). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to use the high-k dielectric material as gate dielectric layer since The increased capacitance k of the gate dielectric material advantage results in an increase in the gate-to-channel capacitance, which in turn results in improved device performance.

Yu teaches suitable electrically conductive materials for use as gate electrode layer include polysilicon or metal (Col.8, lines 15-19). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to

substitute the polysilicon of Takagi with meatl as taught by Yu since polysilicon and metal are art recognized conductive material for gate electrode.

Re claim 14, Takagi teaches the thin semiconductor material comprises Si but thickness of Si. It is an obvious matter of routine experimentation to find the optimal thickness ranges. Generally, difference in thickness will not support the patentability of subject matter encompassed by the prior art unless there is evidence indicating such thickness is critical.

Allowable Subject Matter

8. Claims 3 & 12 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The following is a statement of reasons for the indication of allowable subject matter:

Prior art reference, taken along or in combination, do not teach or render obvious that the stressed semiconductor layer comprises epitaxially growing a second layer of silicon and carbon, layer of silicon and germanium, or a layer of silicon, carbon and germanium, and wherein growing the stressed semiconductor layer comprises growing a material having a thickness of about 100Å to about 5 μm.

Conclusion

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Donghee Kang whose telephone number is 571-272-1656. The examiner can normally be reached on Monday through Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie C. Lee can be reached on 571-272-1732. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Donghee Kang, Ph.D.
Primary Examiner
Art Unit 2811

dhk